Similar to: Diagnosis of Scan Chain Failures Found 200 of 923,142

Sort results by relevance Save results to a Binder Try an Advanced Search
Display results expanded form Search Tips Try this search in The Digital Library
☐ Open results in a new window

Results 1 - 20 of 200 Result page: 1 2 3 4 5 6 7 8 9 10 next
Relevance scale

1 Intermittent Scan Chain Fault Diagnosis Based on Signal Probability Analysis
Yu Huang, Wu-Tung Cheng, Cheng-Ju Hsieh, Huan-Yung Tseng, Alou Huang, Yu-Ting Hung
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 2**
Publisher: IEEE Computer Society
Additional Information: full citation, abstract, index terms

A new algorithm to diagnose intermittent scan chain fault in scan-based designs is proposed in this paper. An intermittent scan chain fault sometimes is triggered and sometimes is not triggered during scan chain shifting, which makes it very difficult to locate the fault sites. In this paper, we provide answers to three questions:(1) Why intermittent scan chain faults happen?(2) Why diagnosis of this type of faults is necessary?(3) How to diagnose this type of faults?The experimental results pre ...

2 Poster session III: Using fault model relaxation to diagnose real scan chain defects
Yu Huang, Wu-Tung Cheng, Greg Crowell
January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**
Publisher: ACM Press
Full text available: pdf(389.96 KB) Additional Information: full citation, abstract, references

Software-based scan chain fault diagnosis is typically composed of two steps. First, scan chain flush patterns are used to identify faulty chains and fault models. This is followed by chain diagnosis using scan patterns in the second step. In this paper, we target chain diagnosis on one special category of chain faults: intermittent scan chain faults. It is showed that these faults may not be modeled correctly in the first step. Hence, a novel diagnosis methodology based on scan chain fault mode ...

3 Diagnosis of scan path failures
S. Edirisooriya, G. Edirisooriya
April 1995 **Proceedings of the 13th IEEE VLSI Test Symposium (VTS'95)**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract, citings

Abstract: Scan based diagnostic schemes are used to diagnose faults in faulty circuits. Such techniques assume that the scan path itself is fault-free. However, the logic circuitry associated with the scan chain may occupy nearly 30% of a chip area and hence warrants consideration during fault diagnosis. In this work we propose a simple extension to the scan chain to diagnose faults in scan chains.

Keywords: combinational circuits, design for testability, fault diagnosis, faulty circuits, integrated circuit testing, integrated logic circuits, logic circuitry, logic testing, scan based diagnostic schemes, scan chain fault diagnosis, scan path failures

4 Diagnosis of Multiple Hold-Time and Setup-Time Faults in Scan Chains

James C. -M. Li

November 2005 **IEEE Transactions on Computers**, Volume 54 Issue 11

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract, references, index terms

This paper presents a diagnosis technique to locate hold-time (HT) faults and setup-time (ST) faults in scan chains. This technique achieves deterministic diagnosis results by applying thermometer scan input (TSI) patterns, which have only one rising or one falling transition. With TSI patterns, the diagnosis patterns can be easily generated by existing single stuck-at fault test pattern generators with few modifications. In addition to the first fault, this technique diagnoses remaining faults ...

Keywords: Index Terms- Fault diagnosis, ATPG, scan chain.

5 Multiple Scan Chain Design Technique for Power Reduction during Test Application in BIST

Debjyoti Ghosh, Swarup Bhunia, Kaushik Roy

November 2003 **Proceedings of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract, index terms

Multiple scan chain has been used in DFT (design for test) architectures primarily to reduce test application time. Since power is an emerging problem, in this paper, we present a design technique for multiple scan chain in BIST (Built-In Self Test) to reduce average power dissipation and test application time, while maintaining the fault coverage. First, we partition the scan chain into a set of smaller chains of similar lengths in such a way, that the total number of scan transitions in the sc ...

6 IEEE 1149.1 Based Defect and Fault Tolerant Scan Chain for Wafer Scale Integration

Meng Lu, Yvon Savaria, Bing Qiu, Jacques Taillefer

November 2003 **Proceedings of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract, index terms

This paper presents an IEEE 1149.1 based defect and fault tolerant scan chain usable for testing and configuring large area and wafer scale integrated systems. It uses the Triple Modular Redundancy (TMR) approach to tolerate defects on critical portions of IEEE1149.1 circuitry. By a suitable distribution of sensitive circuits, failures on power, clock (TCK) and control signals (TMS and nTRST) can be tolerated. Some implementation issues, such as layout regularity and timing are discussed. The yi ...

7 A Technique for Fault Diagnosis of Defects in Scan Chains

Ruifeng Guo, Srikanth Venkataraman

October 2001 **Proceedings of the 2001 IEEE International Test Conference**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract

In this paper,we present a scan chain faultdiagnosis procedure.The diagnosis for a singlescan chain fault is performed in three steps.Thefirst step uses special chain test patterns todetermine both the faulty chain and the fault type inthe faulty chain.The second step uses a novelprocedure to generate special test patterns toidentify the suspect scan cell ithin a range of scancells.Unlike previously proposed methods thatrestrict the location of the faulty scan cell only fromthe scan chain output ...

8 Injecting Bit Flip Faults by Means of a Purely Software Approach: A Case Studied
Raoul Velazco, A. Corominas, P. Ferreyra
November 2002 **Proceedings of the 17th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract

Bit flips provoked by radiation are a main concern for space applications. A fault injectionexperiment performed using a software simulator is described in this paper. Obtained resultsallow to predict a low sensitivity to soft errors for the studied application, putting in evidencecritical memory elements.

9 Partial scan selection for user-specified fault coverage
Clay Gloster, Franc Brglez
December 1995 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(711.12 KB) Additional Information: full citation, references, index terms

10 An Efficient Multiple Scan Chain Testing Scheme
Zaifu Zhang, Robert D. McLeod
March 1996 **Proceedings of the 6th Great Lakes Symposium on VLSI**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract, citings

In this paper an improved multiple scan chain testing scheme to enhance stuck-at and delay fault testing is proposed. With judicial selection of taps from an n stage CA generator, correlation within a multiple input scan chain is reduced. Adopting the multiple scan chains fed by the selected taps of the CA generator also eases the difficulty of arranging shift register latches (SRLs) for scan based pseudo-exhaustive stuck-at fault testing.

11 A Zero Aliasing Built-In Self Test Technique for Delay Fault Testing
Y. Tsiatouhas, Th. Haniotakis
November 1999 **Proceedings of the 14th International Symposium on Defect and Fault-Tolerance in VLSI Systems**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract

A zero aliasing built-in self-test (BIST) approach to detect timing related failures in VLSI circuits is proposed. The BIST scheme is based on a transition detector and is able to detect timing related failures resulting in shorter than expected as well as larger than expected delay faults.

Keywords: Built-In Self Test, Delay Fault Testing

12 Quick Scan Chain Diagnosis Using Signal Profiling

Jheng-Syun Yang, Shi-Yu Huang
October 2005 **Proceedings of the 2005 International Conference on Computer Design - Volume 00 ICCD '05**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract

In this paper we address the scan chain diagnosis problem. We propose a new diagnosis flow based on the concept of signal profiling to accurately pinpoint the location of a faulty flip-flop in a scan chain. As compared to the conventional cause-effect or effect-cause analysis, this approach is much more computationally efficient because it does not have to simulate the behaviors of a large number of fault candidates. Also, it is general and applicable to all kinds of faults because it does not a ...

13 How Seriously Do You Take Possible-Detect Faults?
Rajesh Raina, Charles Njinda, Robert Molyneaux
November 1997 **Proceedings of the 1997 IEEE International Test Conference**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract

Digital designs, implemented in CMOS technology, haveincreasingly used t&state logic (pass gates) to increaseclock speed. It is also known that tri-state logic baseddesigns have poor testability, as measured by the singlestuck-at fault model, due to the proliferation of "possible-detect" faults. Design For Test techniques that havebeen developed to address testability issues with tri-statelogic designs, often incur hardware and cycle-time over-heads.In this paper, we discuss the effect of one cl ...

14 Distance Restricted Scan Chain Reordering to Enhance Delay Fault Coverage
Wei Li, Seongmoon Wang, Srimat T. Chakradhar, Sudhakar M. Reddy
January 2005 **Proceedings of the 18th International Conference on VLSI Design held jointly with 4th International Conference on Embedded Systems Design (VLSID'05) - Volume 00**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract

This paper presents a new technique to improve the delay fault coverage by re-ordering flip-flops in a scan chain. Unlike prior techniques where scan flip-flops can be reordered arbitrarily to form a new scan chain order, we restrict the distance by which a scan flip-flop can be moved to create the new scan chain order. The distance restriction makes it practical to make post-synthesis, local layout modifications to accommodate the new scan chain order. It also minimizes the routing overhead req ...

15 Redundant Faults in TSC Networks: Definition and Removal
Cristiana Bolchini, Fabio Salice, Donatella Sciuto
November 1996 **Proceedings of the 1996 Workshop on Defect and Fault-Tolerance in VLSI Systems**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract, citings

When designing Totally Self-Checking (TSC) systems the user imposes a functional encoding methodology and a constrained synthesis for guaranteeing that each fault produces a detectable error with respect to the applied coding. Both aspects, functional methodology and synthesis constraints, are not always supported by automatic tools thus possibly leading to the presence of undetected faults. The paper presents a classification of redundant faults with respect to TSC circuits (TSC redundant fault ...

16 Novel Berger code checker
C. Metra, M. Favalli, B. Ricco

November 1995 **Proceedings of the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract, citings

This paper presents a novel checking circuit for Berger codes, with any value of k (also k=2/sup r-1/), which is TSC with respect to a wide set of realistic faults including all possible stuck-ats, transistors stuck-on/stuck-open, as well as several likely to occur resistive bridgings. With respect to the other alternative implementations the proposed checker features the advantage of being inherently more testable, and of requiring lower area overhead.

Keywords: Berger codes, TSC, area overhead, checking circuit, error detection codes, failure analysis, fault diagnosis, resistive bridgings, stuck-ats, stuck-on faults, stuck-open faults, totally self-checking

17 Scan Encoded Test Pattern Generation for BIST

Kun-Han Tsai, Janusz Rajski, Malgorzata Marek-Sadowska

November 1997 **Proceedings of the 1997 IEEE International Test Conference**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract

This paper presents an improved scan-based BISTscheme which achieves very high fault coverage withoutany modification of the mission logic, i.e. no test pointinsertion, no test data to store and very simple BIST hardwarewhich does not depend on the size of the circuit. Theapproach utilizes scan order and its polarity in scan synthesis,effectively converting it into a ROM encoding a fewtest vectors which serve as centers of clusters from whichthe other vectors are derived by complementing at rand ...

18 New Methods for Evaluating the Impact of Single Event Transients in VDSM ICs

Dan Alexandrescu, Lorena Anghel, Michael Nicolaidis

November 2002 **Proceedings of the 17th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract, citings

This work considers a SET (single event transient) fault simulation technique to evaluatethe probability that a transient pulse, born in the combinational logic, may be latched in astorage cell. Fault injection procedures and a fast fault simulation algorithm for transientfaults were implemented around an event driven simulator. A statistical analysis wasimplemented to organize data sampled from simulations. The benchmarks show that theproposed algorithm is capable of injecting and simulating a ...

19 Maximum Likelihood Estimation for Yield Analysis

F. Joel Ferguson, Jianlin Yu

November 1996 **Proceedings of the 1996 Workshop on Defect and Fault-Tolerance in VLSI Systems**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract

This paper presents an iterative maximum likelihood (ML) estimation method for statistical analysis of yield loss. By means of Inductive Fault Analysis (IFA) and circuit simulation, the mapping between defect types to the corresponding fault signature is constructed. Using the count of each fault signature occurrence, which is provided by a tester, the most likely causes of low yield are identified automatically without the need for physically deprocessing the defective ICs. We show that our met ...

20 Practical Application of Automated Fault Diagnosis for Stuck-at, Bridging, and Measurement Condition Dependent Faults in Fully Scanned Sequential Circuits

Reisuke Shimoda, Takaki Yoshida, Masafumi Watari, Yasuhiro Toyota, Kiyokazu Nishi, Akira Motohara

November 1999 **Proceedings of the 8th Asian Test Symposium**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract

A practical fault diagnosis system based on combinational Automatic Test Pattern generation (A TPG) and fault simulation is described. Our fault diagnosis system deals with conventional stuck-at and bridging faults, as well as measurements condition dependent (MCI)) faults in order lo diagnose those faults causing different behavior by measurement condition such as supply voltage and temperature, using single stuck-at based diagnosis techniques. experimental results with practical very deep subm ...

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next